AMENDMENTS TO THE SPECIFICATION

Please amend the "Cross-Reference to Related Applications" section on pages 1-3 of the application as follows:

CROSS-REFERENCE TO RELATED APPLICATIONS

The present invention is related to those disclosed in the following United States Patent Applications:

1) Serial No. 09/751,372 ~~[Docket No. 00-BN-051]~~, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR EXECUTING VARIABLE LATENCY LOAD OPERATIONS IN A DATA PROCESSOR";

2) Serial No. 09/751,331 (now U.S. Patent No. 6,865,665) ~~[Docket No. 00-BN-052]~~, filed concurrently herewith, entitled "PROCESSOR PIPELINE STALL APPARATUS AND METHOD OF OPERATION";

3) Serial No. 09/751,371 (now U.S. Patent No. 6,691,210) ~~[Docket No. 00-BN-053]~~, filed concurrently herewith, entitled "CIRCUIT AND METHOD FOR HARDWARE-ASSISTED SOFTWARE FLUSHING OF DATA AND INSTRUCTION CACHES";

4) Serial No. 09/751,327 (now U.S. Patent No. 6,829,700) ~~[Docket No. 00-BN-054]~~, filed concurrently herewith, entitled "CIRCUIT AND METHOD FOR SUPPORTING MISALIGNED ACCESSES IN THE PRESENCE OF SPECULATIVE LOAD INSTRUCTIONS";

5) Serial No. 09/751,377 ~~[Docket No. 00-BN-055]~~, filed concurrently

herewith, entitled "BYPASS CIRCUITRY FOR USE IN A PIPELINED PROCESSOR";

6) Serial No. 09/751,410 ~~[Docket No. 00-BN-056]~~, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR EXECUTING CONDITIONAL BRANCH INSTRUCTIONS IN A DATA PROCESSOR";

now US Patent No. 6,807,628

7) Serial No. 09/751,330 ~~[Docket No. 00-BN-058]~~, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR SUPPORTING PRECISE EXCEPTIONS IN A DATA PROCESSOR HAVING A CLUSTERED ARCHITECTURE";

8) Serial No. 09/751,674 ~~[Docket No. 00-BN-059]~~, filed concurrently herewith, entitled "CIRCUIT AND METHOD FOR INSTRUCTION COMPRESSION AND DISPERSAL IN WIDE-ISSUE PROCESSORS";

now US. Patent No 6,772,355

9) Serial No. 09/751,678 ~~[Docket No. 00-BN-066]~~, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR REDUCING POWER CONSUMPTION IN A DATA PROCESSOR HAVING A CLUSTERED ARCHITECTURE"; and

10) Serial No. 09/751,679 ~~[Docket No. 00-BN-067]~~, filed concurrently herewith, entitled "INSTRUCTION FETCH APPARATUS FOR WIDE ISSUE PROCESSORS AND METHOD OF OPERATION".

The above applications are commonly assigned to the assignee of the present invention. The disclosures of these related patent applications are hereby incorporated by reference for all

purposes as if fully set forth herein.